

RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

FIRST YEAR [2018-21]

B.A./B.Sc. FIRST SEMESTER (July – December) 2018

Mid-Semester Examination, September 2018

Date : 24/09/2018

COMPUTER SCIENCE (Honours)

Time : 11 am – 1pm

Paper: I

Full Marks : 50

[Use a separate Answer Book for each group]

GROUP – A

Answer **any three** questions:

(3 × 5)

1. Define algorithm. State the characteristics of an algorithm. (1+4)
2. a) Write an algorithm to count total number of even digits in a given number. 3
b) When does $p \equiv q$ become true? 1
c) Express “ p NAND q ” by using other logical operators. 1
3. a) What is an XS-3 Gray Code? Give suitable example. 2
b) What is the number of parity bits in a 12-bit Hamming Code? 1
c) Code AK47 in ASCII. 1
d) Detect and correct error, if any, in the even parity Hamming Code word “0111110” and write the correct code. 1
4. a) Draw a logic diagram that implements
$$A = (X_1 \odot X_2) \oplus (X_3 \odot X_4) + (X_4 \oplus X_5) \odot (X_6 \oplus X_7).$$
 3
b) Define absorption law. 1
c) State De Morgan’s theorem. 1
5. a) What is principle of duality? 2
b) Show that
$$A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$$
 2
c) Which logical operators form a functionally complete set and why? 1

GROUP – B

Answer **any five** questions:

(5 × 7)

6. a) What is the decimal equivalent value of 11000011 in
 - (i) Unsigned integer representation.
 - (ii) Signed 2’s complement representation.
 - (iii) Signed integer representation.

- b) Perform $(7)_{10} \div (2)_{10}$ using restoring division method. Also draw the flowchart for the operation. 4+3
7. a) Design a 1-bit magnitude comparator circuit.
- b) Perform $X = ((A + B) * C) / D$ using one address and zero address instruction format. 3+4
8. a) A computer has an 4GB of memory with 64 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. What is the address format?
- b) Derive the characteristic equation of a S-R flip-flop. 3+4
9. a) Design a combinational logic circuit to produce the 2's complement of a 3-bit binary number.
- b) Implement a full subtractor using a suitable decoder and necessary logic gates.
- c) What is implied or implicit addressing mode? 3+3+1
10. a) Draw and explain data flow of fetch cycle in brief.
- b) Implement the following logic function:

$$F(x, y, z) = x \oplus y \oplus z$$
using a 4:1 multiplexer. 4+3
11. a) How can a demultiplexer be realized using a decoder?
- b) Write the practical uses of various types of ROMs.
- c) Design 128×8 RAM using 32×8 RAMs and other necessary logic gates or decoders. 2+2+3
12. a) Design a combinational logic circuit with four inputs A, B, C and D that will produce output 1 only when two adjacent input variables are 1's. A and D are also to be treated as adjacent.
- b) What is bus arbitration?
- c) Why is address bus bidirectional? 3+2+2

_____ × _____